

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A static flip-flop circuit comprising:

a master circuit comprising a first data reading circuit~~differential pair~~, a first data-hold ~~differential pair~~circuit ~~comprising~~composed of transistors of a size smaller than transistors ~~comprising~~constituting the first data reading ~~differential pair~~circuit, and a first current source circuit connected to the first data reading ~~differential pair~~circuit and the first data-hold ~~differential pair~~circuit; and

a slave circuit comprising a second data reading ~~differential pair~~circuit, a second data-hold ~~differential pair~~circuit ~~comprising~~composed of transistors of a size smaller than transistors ~~comprising~~constituting the second data reading ~~differential pair~~circuit, and a second current source circuit connected to the second data reading ~~differential pair~~circuit and the second data-hold ~~differential pair~~circuit;

~~wherein the flip-flop circuit operates in an operating speed range in which the currents through the first and second data-hold differential pairs are lower than the currents through the first and second data reading differential pairs, and the currents through the first and second data-hold differential pairs are equal to or lower than the permissible current level of the transistors that constitute the data-hold differential pairs~~

wherein, since a size of the transistors constituting the first and second data-hold circuit is smaller than a size of the transistors constituting the first and second data reading circuit, in the working operation range, it causes a difference to the currents flowing through the first and second data-hold circuits and the currents flowing through the first and second data reading circuits, and thereby, the currents flowing through the first and second data-hold circuits are lower than the currents flowing through the first and second data reading circuits.

2. (withdrawn) A static flip-flop circuit characterized in that it comprises:

a master circuit including a first data reading differential pair, a first data-hold differential pair composed of transistors of a size smaller than the transistors constituting the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair;

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of transistors of a size smaller than the transistors constituting the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair; and

a current control terminal connected to the first and second current source circuits for controlling the currents through the first and second data reading differential pairs and the currents through the first and second data-hold differential pairs, in accordance with the operating speed of the flip-flop circuit.

3. (withdrawn): The static flip-flop circuit according to Claim 2, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the current control terminal adjusts the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

4. (withdrawn): A static flip-flop circuit characterized in that it comprises:

 a master circuit including a first data reading differential pair, a first data-hold differential pair composed of transistors of a size smaller than the transistors constituting the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair;

 a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of transistors of a size smaller than the transistors constituting the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair;

 a first integrating circuit interposed between the first current source circuit for the master circuit and the terminal to which a clock signal is input; and

a second integrating circuit interposed between the second current source circuit for the slave circuit and the terminal to which a complementary clock signal is input.

5. (withdrawn): The static flip-flop circuit according to Claim 4, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second integrating circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

6. (withdrawn): A static flip-flop circuit characterized in that it comprises:
a master circuit including a first data reading differential pair, a first data-hold differential pair composed of transistors of a size smaller than the transistors constituting the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair;

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of transistors of a size smaller than the transistors constituting the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair;

a first low-pass filter circuit interposed between the first current source circuit for the master circuit and the terminal to which a clock signal is input; and

a second low-pass filter circuit interposed between the second current source circuit for the slave circuit and the terminal to which a complementary clock signal is input.

7. (withdrawn): The static flip-flop circuit according to Claim 6, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second low-pass filter circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

8. (withdrawn): A static flip-flop circuit characterized in that it comprises:

a master circuit including a first data reading differential pair, a first data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the transistors constituting the first data reading differential pair, and connected to each other in parallel via a first low-pass filter circuit, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair; and

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the

transistors constituting the second data reading differential pair, and connected to each other in parallel via a second low-pass filter circuit, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair.

9. (withdrawn): The static flip-flop circuit according to Claim 8, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second low-pass filter circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

10 (withdrawn): A static flip-flop circuit characterized in that it comprises:

a master circuit including a first data reading differential pair, a first data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the transistors constituting the first data reading differential pair, and connected to each other in parallel via a first circuit including inductance, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair; and

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the transistors constituting the second data reading differential pair, and connected to each other in

parallel via a second circuit including inductance, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair.

11. (withdrawn): The static flip-flop circuit according to Claim 10, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

12. (withdrawn): The static flip-flop circuit according to any one of Claims 4, 6, 8 and 10, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the currents through the first and second data-hold differential pairs are adjusted to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs, depending on the operating speed.

13. (previously presented): The static flip-flop circuit according to Claim 1, wherein, when operating speed of the flip-flop circuit lowers from the maximum operating speed, the currents through the first and second data-hold differential pairs increase, and at the minimum operating speed the current through the first data-hold differential pair becomes equal to the current through the first data reading differential pair and the current through the second data-

hold differential pair becomes equal to the current through the second data reading differential pair.

14. (previously presented): The static flip-flop circuit according to Claim 1, wherein the sum of the current through the first data-hold differential pair and the current through the first data reading differential pair is equal to the current of the first current source circuit, and the sum of the current through the second data-hold differential pair and the current through the second data reading differential pair is equal to the current of the second current source circuit.

15. (new): The static flip flop circuit according to claim 1, wherein the current flowing through the first and second data-hold circuits is equal to or lower than the permissible current level of the transistors that constitute the data-hold circuits.